

N-Channel 60-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4436 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

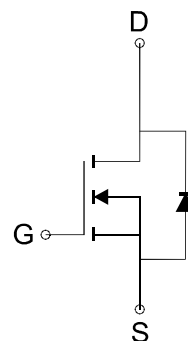
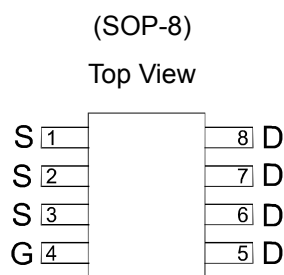
FEATURES

- $R_{DS(ON)} \leq 33m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 40m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter

PIN CONFIGURATION



N-Channel MOSFET

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DSS}	60		V
Gate-Source Voltage		V _{GSS}	±20		
Continuous Drain	T _A =25°C	I _D	8.6	6.9	A
Current(T _J =150°C)	T _A =70°C		6.4	5.1	
Pulsed Drain Current		I _{DM}	30		
Continuous Source-Drain Diode Current		I _S	2		
Avalanche Current	L=0.1mH	I _{AS}	15		
Single-Pulse Avalanche Energy		E _{AS}	12		mJ
Maximum Power Dissipation	T _A =25°C	P _D	6.4	5	W
	T _A =70°C		5.1	4	
Operating Junction & Storage Temperature Range		T _J	-55 to 150		°C
Thermal Resistance-Junction to Ambient *		RθJA	46	76	°C/W
Thermal Resistance-Junction to Case *		RθJC	43		

*The device mounted on 1in² FR4 board with 2 oz copper

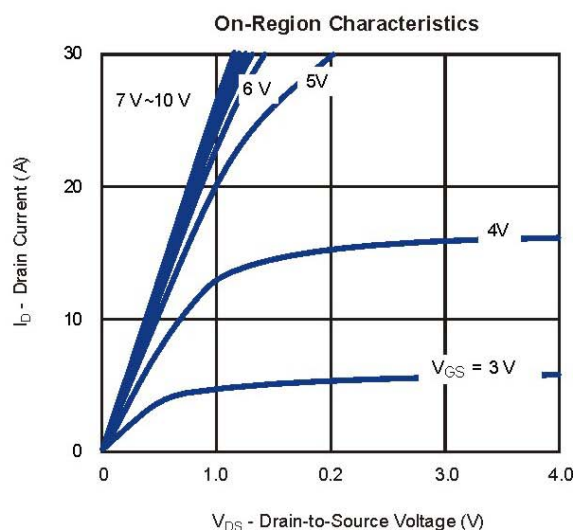
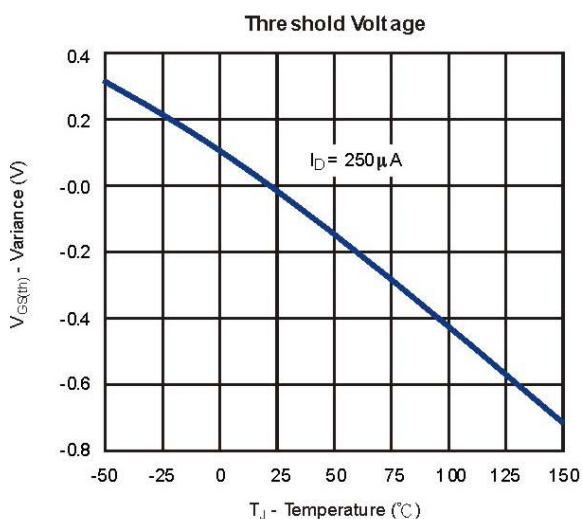
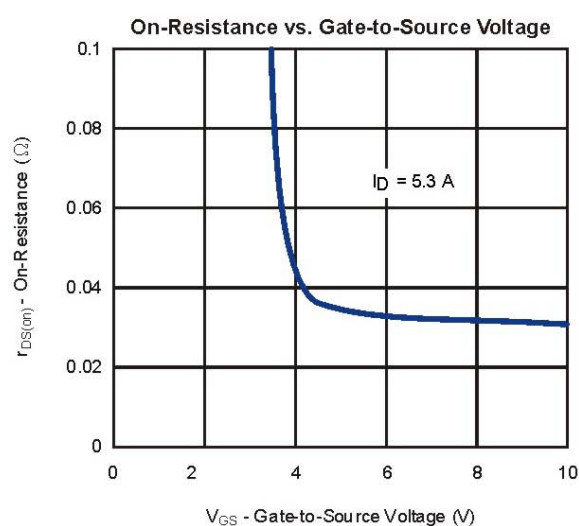
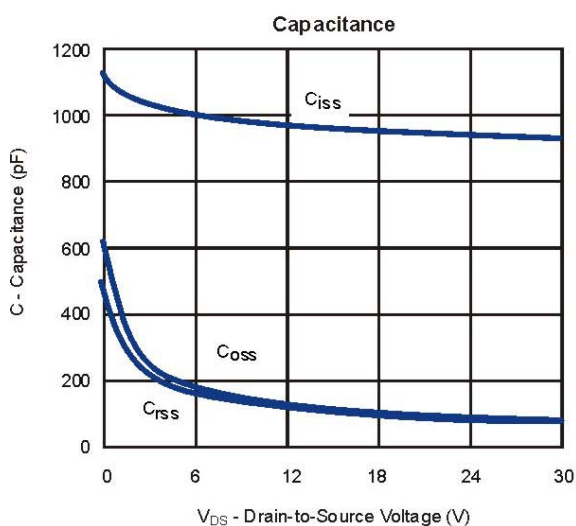
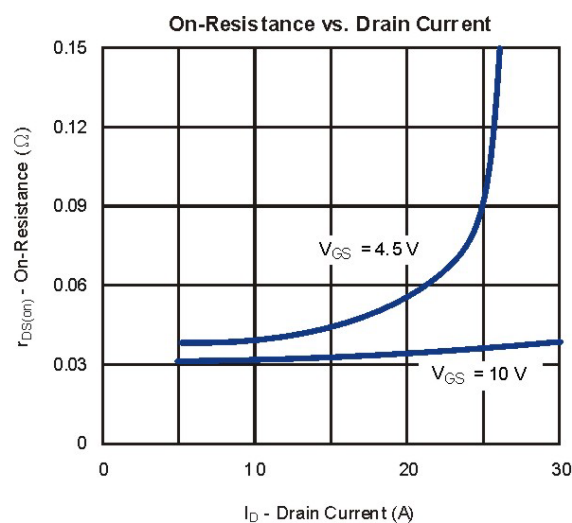
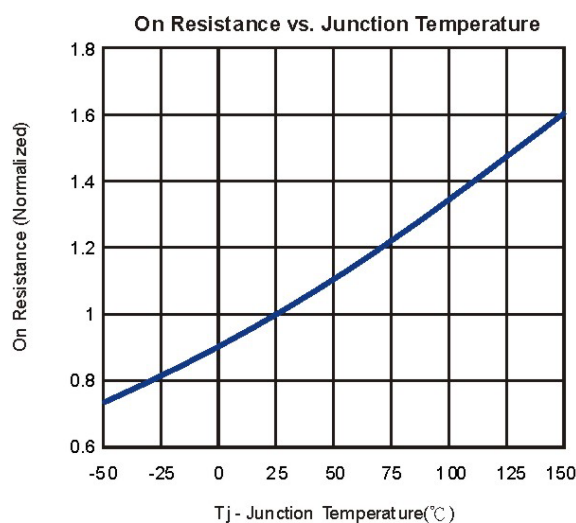
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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC						
V _{DS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1.0	1.8	3.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V			1	μA
		V _{DS} =60V, V _{GS} =0V			10	
		T _J =55°C				
I _{D(ON)}	On-State Drain Current ^a	V _{DS} ≥5V, V _{GS} =10V	30			A
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D = 5.3A		26	33	mΩ
		V _{GS} =4.5V, I _D = 4.7A		31	40	
V _{SD}	Diode Forward Voltage	I _S =2A		0.8	1.2	V
DYNAMIC						
C _{iss}	Input capacitance	V _{DS} =30V, V _{GS} =0V, f=1.0MHz		940	1100	pF
C _{oss}	Output Capacitance			71		
C _{rss}	Reverse Transfer Capacitance			33		
Q _g	Total Gate Charge	V _{DS} =30V, V _{GS} =10V, I _D =5.3A		22	29	nC
				13.3	18	
Q _{gs}	Gate-Source Charge	V _{DS} =30V, V _{GS} =5V, I _D =5.3A		7.1		
Q _{gd}	Gate-Drain Charge			7.5		
R _g	Gate Resistance	f=1MHz		0.9		Ω
t _{d(on)}	Turn-On Delay Time	V _{DD} =30V, R _L =6.8Ω I _D =4.4A, V _{GEN} =10V R _G =1Ω		14	18	ns
t _r	Turn-On Rise Time			26	33	
t _{d(off)}	Turn-Off Delay Time			41	52	
t _f	Turn-Off Fall Time			3.6	6	
t _{d(on)}	Turn-On Delay Time	V _{DD} =30V, R _L =6.8Ω I _D =4.4A, V _{GEN} =4.5V R _G =1Ω		12	16	
t _r	Turn-On Rise Time			26	33	
t _{d(off)}	Turn-Off Delay Time			42	52	
t _f	Turn-Off Fall Time			3.8	7	

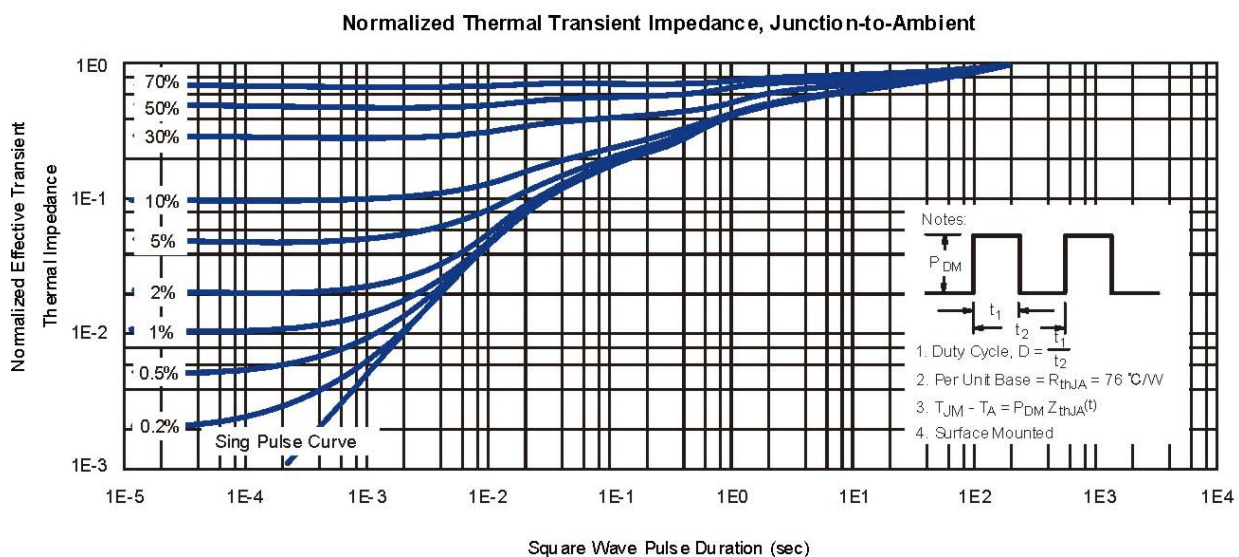
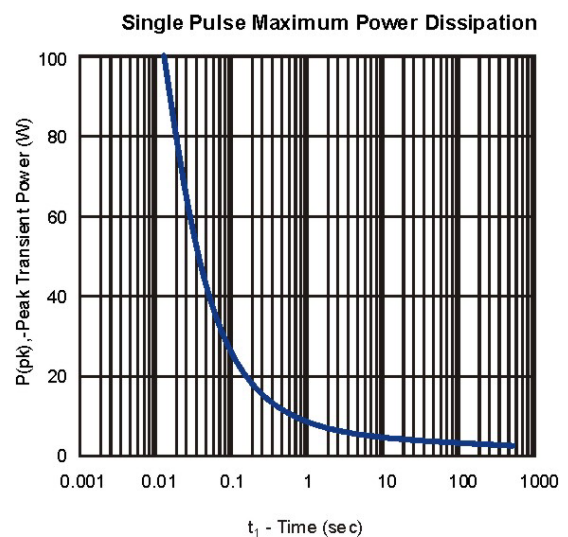
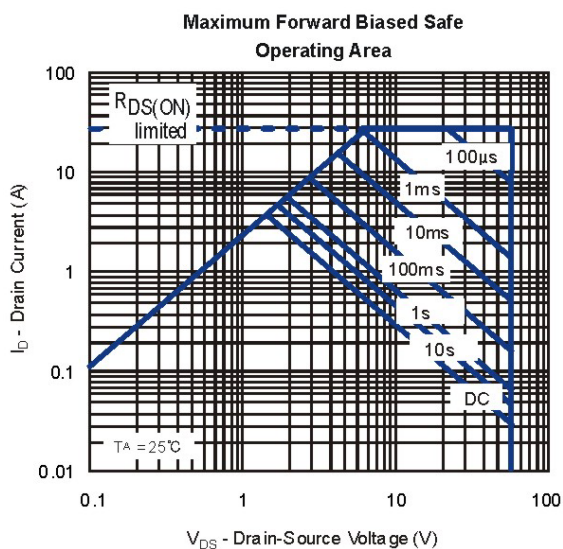
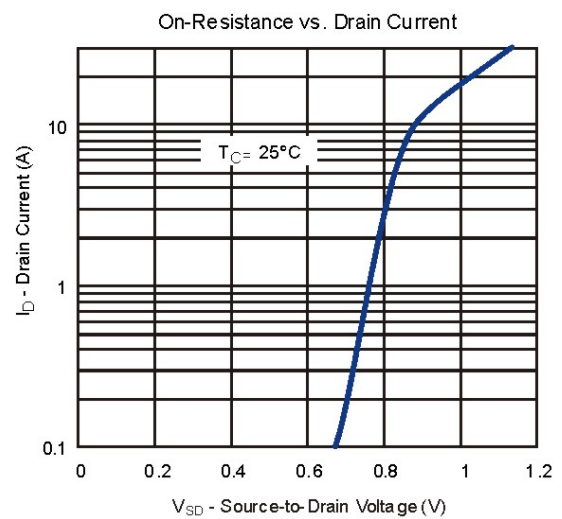
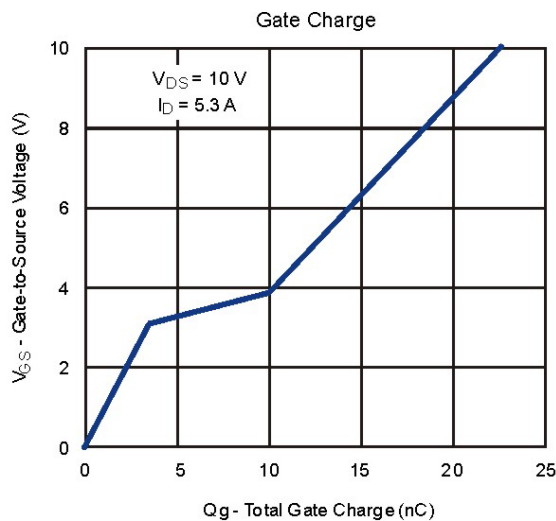
Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

Typical Characteristics (T_J = 25°C Noted)



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Typical Characteristics (T_J = 25°C Noted)



SOP-8 Package Outline

